ABSTRACT OF THE DISCLOSURE

Semiconductor processing methods of forming integrated circuitry are described. In one embodiment, memory circuitry and peripheral circuitry are formed over a substrate. The peripheral circuitry comprises first and second type MOS transistors. Second type halo implants are conducted into the first type MOS transistors in less than all of the peripheral MOS transistors of the first type. In another embodiment, a plurality of n-type transistor devices are formed over a substrate and comprise memory array circuitry and peripheral circuitry. At least some of the individual peripheral circuitry n-type transistor devices are partially masked, and a halo implant is conducted for unmasked portions of the partially masked peripheral circuitry n-type transistor devices. In yet another embodiment, at least a portion of only one of the source and drain regions is masked, and at least a portion of the other of the source and drains regions is exposed for at least some of the peripheral circuitry n-type transistor devices. A halo implant is conducted relative to the exposed portions of the source and drain regions. In another embodiment, a common masking step is used and a halo implant is conducted of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages.